

UNITED STATES PATENT APPLICATION

FOR

SYSTEM AND METHOD FOR BUILT-IN TESTING OF A GPS RECEIVER

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SYSTEM AND METHOD FOR BUILT-IN TESTING OF A GPS RECEIVER

FIELD OF THE INVENTION

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The present claimed invention relates to the field of global positioning system (GPS) instruments. More particularly, the present claimed invention relates to built-in testing of GPS instruments.

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BACKGROUND ART

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In civil aircraft operations where system safety is a paramount concern, it is important that GPS receivers not be allowed to operate in a defective fashion that outputs potentially hazardous and misleading information (HMI) to a pilot. Thus, the probability of a GPS receiver outputting such information is typically specified (e.g., less than 10^{-5} per flight hour) by regulations governing civil aviation.

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The Federal Aviation Administration (FAA) has developed certification procedures for GPS airborne receivers using the Standard Positioning Service (SPS) for Instrument Flight Rules (IFR) operation in the National Airspace System (NAS), embodied in Technical Standard Orders (TSOs) C129a, C145, and C146. The certification of a GPS airborne receiver depends in part on its built-in test (BIT) capability.

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As GPS receivers become more complex, the difficulty in achieving sufficient test coverage increases. For example, military GPS receivers may have Selective Availability/Anti-Spoof Module (SAASM) capability, or M-Code processing
5 capability.

SAASM and M-code technologies require additional components for signal processing and computation that may be employed in either the analog or digital portions of the
10 signal path of a GPS receiver, and must be accounted for in a system providing a complete built. However, the ability to provide built-in testing of these technologies is lacking in the prior art.

15 Thus a need exists for a system and method for testing a GPS receiver that provides an improved BIT capability. There is also a need for system and method that provides a BIT capability for both the analog and digital portions of the signal path in a GPS receiver.

SUMMARY OF INVENTION

Accordingly, the present invention provides a system and method for built-in testing of a global positioning system (GPS) receiver. Embodiments of the present invention provide a loop forward capability and a loop backward capability that in combination provide a comprehensive BIT capability for both the analog and digital portions of the signal path in a GPS receiver.

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In one embodiment built-in test equipment (BITE) incorporated in a GPS receiver performs a loop forward test that generates deterministic GPS test data which are used to modulate one or more RF carriers to produce RF test signals.

15 The RF test signals are applied to the GPS receiver's radio frequency (RF) front end. These signals are then processed through an operational signal path of the GPS receiver and compared to the initial test data.

20 In another embodiment, a loop backward BITE is used by a system processor in a GPS receiver to sample the positioning data and output by the GPS receiver. The microprocessor also controls a loop forward BITE, thus providing comprehensive testing of the signal path within the GPS receiver.

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BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

Figure 1 shows a circuit block diagram for a portion of a GPS receiver including RF analog circuitry, a Selective Availability/Anti-Spoof Module (SAASM), and loop forward built-in test equipment (BITE) in accordance with an embodiment of the present claimed invention.

Figure 2 shows a modular diagram for a GPS receiver in accordance with an embodiment of the present claimed invention.

Figure 3 shows a block diagram for data flow in a GPS receiver including loop forward BITE and loop backward BITE in accordance with an embodiment of the present claimed invention.

Figure 4A shows a flow diagram for a method of performing loop forward built-in testing of a GPS receiver in accordance with an embodiment of the present claimed invention.

Figure 4B shows a flow diagram for a method of performing loop backward built-in testing of a GPS receiver accordance with an embodiment of the present claimed invention.

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DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred
5 embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within
10 the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be
15 obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

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Figure 1 shows a circuit block diagram for a portion of a GPS receiver 100 including a Selective Availability/Anti-Spoof Module (SAASM) 130, and loop forward built-in test equipment (BITE) in accordance with an embodiment of the
25 present invention.

An RF input stage 115 accepts radio frequency (RF) GPS signals from an antenna (not shown). The RF input stage 115 includes a diplexer for separating the L1 (1575.42MHz) and L2 (1227.6MHz) signals, and may also provide gain for the L1 and L2 signals. A filter/converter 116 provides filtering and downconversion of the L1 signal and an AGC/converter 118 provides automatic gain control and further downconversion of the L1 signal to an intermediate frequency (IF). The filter/converter 117 and AGC/converter 119 perform similar functions for the L2 signal, as described for the L1 signal.

The IF signals derived from L1 AGC/converter 118 and the L2 AGC/converter 119 are input to an L1 analog-to-digital converter (ADC) 120 and an ADC 121, respectively. L1 ADC 120 and L2 ADC 121 each produce an IF digital signal. A reference oscillator 125 is used to provide the reference frequencies for converters 116, 117, 118, 119, and is also used to provide the clock signal for L1 ADC 120 and L2 ADC 121. The reference oscillator may also be used to generate reference signals for the RF BIT modulator 185, as well as clock signals for digital circuits such as the code generator 155.

The digital IF signals from the L1 ADC 120 and the L2 ADC 121 are input to the SAASM module 130. The SAASM module 130 provides among other functions, the capability to directly acquire P(Y) Code, enabling a GPS receiver to use

the Precise Positioning Service (PPS) without requiring the coarse acquisition (C/A) code.

Traditionally, the PPS has relied on the use of the C/A
5 code in order to obtain access to the P(Y) Code information. For national security purposes selective availability (SA) can be used to degrade the C/A code signal without affecting the PPS. However, the degradation of the C/A code signal using SA is global in extent and cannot be applied locally.

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In the year 2000 SA was turned off, and the increased accuracy available further encouraged civilian adoption of GPS. Although SA could be turned on again if needed, the global impact could unnecessarily affect civilian use. As an
15 alternative to SA, local denial of the C/A code has been introduced as a method of restricting GPS availability to authorized users in a particular region. Since local denial of the C/A code affects all users in a region, authorized users must have the capability to directly acquire the P(Y)
20 code.

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Until recently a very accurate clock was required for direct acquisition of the P(Y) code signal. However, advances in signal processing and integrated circuits has made P(Y)
25 code signal acquisition achievable through intensive calculations without requiring an accurate time. The SAASM 130 provides the signal processing and computational

capability required for direct acquisition of the P(Y) code signal. The SAASM also includes a key data processor for handling cryptographic data processing of the acquired P(Y) code signal.

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The SAASM 130 is coupled to a dual-port random access memory (DPRAM) interface 150 that is in turn coupled to system data bus 160 and an address/control bus 165. The data bus 160 and address/control bus are also coupled to a static
10 random access memory (SRAM) 145, an electrically-erasable programmable read-only memory (EEPROM) 140, a system central processing unit (CPU) 135, and a code generator 155.

The CPU 135 computes position, velocity and time based
15 upon the raw data received from the SAASM 130. The CPU also provides provide overall control of the monitoring and BIT capability of the GPS receiver. A BIT ADC 170 provides data derived from system DC power sources to the CPU 135. Examples
20 of DC levels 175 that may be monitored by the ADC 170 are antenna preamplifier current and voltage, battery voltage, primary power supply voltage, and internal supply voltage (V_{cc}) for on-board devices.

The SAASM module 130 adds considerable complexity to a
25 GPS receiver, and thus increases the both the potential for failure and the need for expanded test coverage.

The code generator 155 provides the digital test data used for testing data processing functions within the GPS receiver. The code generator 155 may be implemented as a field programmable gate array (FPGA), application specific
5 integrated circuit (ASIC), or other integrated circuit. In a system including a sufficiently powerful CPU 135 and available memory for storing instructions, the code generator may be implemented by the CPU 135.

10 The code generator produces test data sequences for both the C/A code and P code. The test sequences are preferably known, deterministic test patterns that can subsequently be compared to a test output to verify system operation. In other embodiments, the code generator 155 may produce a
15 pseudo M code test sequence that is representative of the broadcast M code signal.

The pseudo M code signal uses the L1 and L2 bands, and can be used in conjunction with the C/A code and Y code
20 signals. The pseudo M code signal uses different keying architecture and modulation than the current Y code, and is expected to provide greater flexibility and better performance for military users.

25 In general, the code generator 155 generates one or more sequences of bits that emulate a set or subset of data in accordance with one or more GPS data message formats. These

test sequences (e.g., P code and C/A code) are combined by a bit code combiner 180 and passed to a RF BIT modulator 185.

5 The RF BIT modulator produces one or more RF signals that contain the combined test bit sequences and is modulated using the appropriate scheme. For example, an L1 carrier may be modulated to transmit the P code and/or C/A code and an L2 carrier may be modulated to transmit the P code and/or C/A code.

10

In general, The RF BIT modulator 185 generates one or more RF carrier signals and modulates the carrier signals using the test bit sequences provided by the BIT code combiner 180 to produce BIT RF test signals. The RF BIT
15 modulator may modulate carriers at two different frequencies with the same information, or may modulate two distinct carriers at the same frequency using different bit sequences (e.g., pseudo M code).

20

The BIT RF signal output from the RF BIT modulator 185 and an antenna input 105 are coupled to the RF input stage 15 by a directional coupler 110. The directional coupler 110 minimizes the amount of test signal energy leaked to the antenna, and maximizes the energy input to the RF input stage
25 115. Alternatively, a switch may be used to select between the antenna input 105 and the RF BIT modulator 185.

Three types of BIT may be performed by the GPS receiver. Power-up BIT is conducted when the receiver is first turned on, prior to normal operation. Initiated BIT is performed on demand, and may be performed at any time during normal
5 operation. For power-up BIT and initiated BIT the antenna input may be switched off. Continuous BIT may be performed periodically during normal operation of the GPS receiver. Under continuous BIT, it is desirable that the test signal is not confused with a real signal if continuous testing is
10 performed without switching out the antenna.

In one embodiment, the test signal is distinguished from the real signals by shifting the test signal frequency outside of the expected range of the real signals. In another
15 embodiment the test signal uses a pseudo random noise (PRN) code that is not used by real signal sources. For example, PRN 32 is not used by GPS satellites and may be dedicated to the test signal. The PRN of an operational satellite may be used for a test signal when the satellite is known to be
20 sufficiently below the horizon, so that a real signal cannot be received from the satellite.

For power-on test and initiated test as many as all available receiver channels (e.g., twelve) may be tested
25 since normal operation is suspended. The ability to provide the same signal level to each channel provides a channel

comparison that cannot be made when using multiple transmitted sources.

5 The injection of synthesized L1 and L2 signals from the RF BIT modulator 185 also provides the capability for measurement of and correction for system delay differences between the L1 and L2 signal paths within the GPS receiver. The use of a master clock within the receiver provides precise synchronization between the test signal generator and
10 the receiver channels.

Figure 2 shows a modular diagram 200 for a GPS receiver in accordance with an embodiment of the present invention. A power supply/input/output (PSIO) board 205 has an input 215
15 for system power, a bidirectional data port 220, and a key fill port 225.

The power input 215 provides basic electrical power for the GPS receiver that is conditioned by the PSIO board 205 to
20 provide power for the circuits of the PSIO board 205 and the receiver board 210.

The data port 220 provides external communication for the GPS receiver. For example, the data port 220 may be
25 coupled to a flight management system (FMS). The PSIO board typically provides formatting and/or buffering for the data transmitted and received from the data port 220.

The optional key fill port 225 provides for loading of cryptographic key data. For receivers with a SAASM capability or other restricted technology, one or more keys may be
5 required for enablement and access.

Power 235 is provided to the receiver board 210 over one or more cables. Similarly, data 240 is passed between the receiver board and PSIO board using one or more data cables.
10 The receiver board 230 includes an antenna input 230 for accepting an RF input signal.

Figure 3 shows a block diagram 300 for data flow in a GPS receiver including loop forward BITE and loop backward
15 BITE in accordance with an embodiment of the present invention. The overall data flow occurs between an RF antenna input 305 and a positioning data output 335.

A system processor 325 provides a nexus that joins two
20 halves of the operational signal path of the GPS receiver. The system processor 325 is coupled to loop forward BITE 340 and to loop backward BITE 345. The combination of the system processor 325, loop forward BITE 340, and the loop backward BITE 345 provides test coverage for the GPS receiver from
25 input to output.

Under control of the system processor 325, the loop forward BITE 340 generates an RF signal that is coupled to the RF input 305 of the GPS receiver. The RF input 305 is coupled to an analog processing block 308. In this example
5 the analog processing block 308 includes an L1 path 310 and an L2 path 315. In general, the analog processing block 308 provides functions such as gain, attenuation, filtering, frequency conversion, and analog-to-digital conversion. The output of the analog processing block 308 is typically a
10 digital IF signal.

The analog processing block 308 is coupled to a digital signal processor (DSP) 320. The DSP 320 receives the digital IF signal that typically includes information from multiple
15 sources (e.g., multiple satellites). The DSP 320 provides signal separation, correlation, and produce raw data that may be used by the system processor 325. The DSP 320 may also provide cryptographic functionality.

20 The system processor 325 uses the raw data from the DSP 320 and optional correction data to produce position, time, and velocity information. This information is typically formatted as a digital data message according to a standard protocol.

25

The message from the system processor 325 is passed to an I/O block 330. The I/O block 330 provides an external

communications interface and manages the flow of data into and out of the GPS receiver. The data message may be formatted according one or more communications protocols and is output at a data port 335.

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The loop forward BITE 340 accepts test data from the system processor 325 and converts the data to one or more RF signals that are input to the analog processing block 308. The test data provided by the system processor may be emulate
10 a satellite data message, or it may be a predetermined sequence of bits that does not correspond to a satellite signal.

The test data message may be specific to a specific
15 channel, or it may applied identically to multiple channels. A single signal applied to one or more channels identically provides identical input levels between channels. This circumstance is seldom observable during normal operation, and provides the ability to evaluate the relative performance
20 between channels. In general, a group of test signals may be provided to the receiver front end with each receiver channel being able to independently track a desired test signal.

The deterministic nature of the test data allows to
25 system processor 325 to evaluate the impact of both the analog processing block 308 and the DSP 320 on data integrity.

The loop backward BITE 345 is coupled to the output data port 335 and allows the system processor 325 to sample the output data and compare it to the data that was input to the I/O block 330. The loop backward is distinguished from the loop forward in that the system processor is inherently aware of the signal being input to the I/O block 330. Thus, a specific test data message may or may not be used in the loop backward test.

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Individually and in combination, the loop forward BITE 340 and loop backward BITE 345 provide an increased capability to detect malfunctions in a GPS receiver through BIT. This increased capability is particularly useful in applications where two or more GPS receivers are used in a redundant configuration for backup.

Although the addition of BITE circuitry slightly increases the probability of component failure in the receiver to which it is being added, it significantly improves ability to detect a failure, and appropriately make use of the backup capability that is available in a redundant system.

25 Figure 4A shows a flow diagram 400 for a loop forward portion of a method of performing built-in testing of a GPS receiver accordance with an embodiment of the present

invention. Reference will be made to the GPS receiver front end shown in Figure 1 and data flow of Figure 3; however, the method is not limited to practice with the architectures shown.

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At step 405, a test data message is provided. The test data message may be generated by a code generator (e.g., FPGA) under the control of a system processor within the GPS receiver. The test data message may emulate C/A code, P code, pseudo M code, or other GPS signal.

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At step 410, one or more RF carrier signals are generated. For example, an L1 carrier and an L2 carrier may be generated. Two distinct carrier signals may be generated at a single frequency, or they may generated at different frequencies.

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At step 415, one or more of the carrier signals generated in step 410 are modulated using the test data message of step 405 to produce an RF test signal. The test signal may be a combination signals carrying different codes (e.g., C/A code, P code, pseudo M code).

20

At step 420, the RF test signal(s) are coupled to the RF input of the GPS receiver. The signal(s) may be coupled by a switch or a directional coupler.

25

At step 425, analog processing of the RF test signal(s) is performed. filtering, frequency conversion, gain, attenuation and analog-to-digital conversion may be performed on the RF test signal(s).

5

At step 430, digital processing of the test signal is performed. Channel separation, correlation and cryptographic functions may be performed during digital processing.

10 At step 435, the digitally processed signal is compared to the input test data message. A deviation from the expected result indicates an error in either the operational signal chain or the BITE circuits, and a warning may be issued as to the possibility of hazardous and misleading information
15 (HMI). Steps 405 through 435 provide a loop forward BIT that can be performed by a system processor and BITE circuits such as those shown in Figure 1.

Figure 4B shows a loop backward method 402 of performing
20 built-in testing of a GPS receiver accordance with an embodiment of the present invention. At step 440 positioning data is provided. This may be operational data obtained during normal operation of the GPS receiver, or it may be data specifically generated for test purposes by a system
25 processor.

At step 445, the positioning data is formatted for output transmission (e.g., by I/O block 330 of Figure 3). The output format may be for a specific system such as a flight management system (FMS) or it may be for a general network or
5 bus protocol.

At step 450, the data is transmitted over the output data port (e.g., 335 of Figure 3). At step 455, the output data is sampled. The sampling of the output data may be
10 performed during normal operation, without interruption, or it may be performed during suspended operation using specific test data.

At step 460 the sampled data is compared to the original
15 data. A discrepancy between the sampled data and the original data indicates an error in the normal signal path or the BITE. In either case, and a warning may be issued as to the possibility of hazardous and misleading information (HMI) being output by the GPS receiver.

20 The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations
25 are possible in light of the above teaching. The embodiments

were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications
5 are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.